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# Sparsity-Aware Reconfigurable-precision SAR ADC for mixed-signal computing and ML

**Reconfigurable ADC cutting ML power use 2x while preserving accuracy in edge devices.**

Researchers at Purdue University have developed an energy efficient and lower latency SAR ADC for machine learning (ML) applications. Energy and latency savings are achieved by dynamically leveraging workload sparsity to reconfigure precision without impacting the application accuracy. Compared to other state of the art solutions, testing shows accuracy improvements of up to 5% while reducing power consumption by 1.5-2.2x. This method is different from other approaches as it can actively adjust the ADC precision based on need rather than keeping it constant. This technology can also be integrated into existing platforms.

### Advantages

- Energy and latency savings

- Dynamic adjustment of ADC precision

- No degradation of application accuracy

- Can be integrated into existing platforms

### Applications

- Machine learning

- Mixed-Signal computing

### Technology Validation:

This technology has been validated through testing of a prototype and comparison against state-of-the-art solutions.

Related Publications:

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**Category**
Semiconductors/IC Design & EDA Tools

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M. Ali, I. Chakraborty, U. Saxena, A. Agrawal, A. Ankit and K. Roy, "A 35.5-127.2 TOPS/W Dynamic Sparsity-Aware Reconfigurable-Precision Compute-in-Memory SRAM Macro for Machine Learning," IEEE Solid-State Circuits Letters, vol. 4, pp. 129-132, 2021, doi: 10.1109/LSSC.2021.3093354.

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