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Memory Read Bit Line Amplifier Using a Modified Differential Pair Construct

A new logic-compatible memory architecture dramatically cuts power consumption by up to 96% and nearly doubles memory capacity while maintaining fast read access times for static and dynamic RAM applications.

The memory industry is continuously seeking to improve the attributes of power consumption, read access time, and memory capacity. Power consumption consists of read, write, restore, and refresh power, which are affected by noise sensitivity, retention time, leakage, and threshold voltage. Subsequently, a tradeoff exists when one of these components increases at the expense of another attribute.

Researchers at Purdue University have developed a logic-compatible memory architecture that effectively circumvents the traditional power structure process and reduces power requirements, often by an order of magnitude. This technology is applicable to either static or dynamic RAM and nearly doubles memory capacity while maintaining comparable read access times. By eliminating the effect of die-to-die threshold voltage variation and lowering the write bit line voltage, this technology creates a power savings of 96 percent.

Advantages:

-The predetermined threshold for the bit line amplifier can be adjusted globally

-Static power for each bit line amplifier can be kept low while waiting

-The timing performance is superior to other types of memory sense amplifiers

Potential Applications:

-Static or dynamic RAM

-Computer technology

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Category
Semiconductors/Devices & Components

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