

# Massively Parallel Nanolithography Using Localized Electron Emission

**A novel maskless lithography technology uses focused optical energy to generate massively parallel electron beams, enabling high-resolution, high-speed, and lower-cost semiconductor chip manufacturing.**

Optical lithography, the process of transferring geometric shapes on a mask to a wafer, has been the critical enabling step for determining nanotechnology device performances such as the transistor density and speed in microprocessors. Tools currently used to transfer fixed geometric patterns on a mask to wafers in the production of semiconductor chips cost more than \$50 million each, and the mask cost far outweighs the cost of tools. Designed to match chip capabilities with Moore's Law, next generation tools will be far too costly for both industry and scientists. Researchers have focused on developing massively parallel electron beam lithography and achieved 2 to 3 orders of magnitude throughput enhancement using a variety of methods, but the roadblock has been the lack of an enabling technology to generate millions of high-quality electron beamlets with satisfactory brightness and uniformity. In addition, the current process cannot meet long-term demand to produce faster chips with more functions.

Researchers at Purdue University have developed a new technology that utilizes a novel device to focus optical energy at nanoscale and locally excite electrons to form massively parallel electron beams, which can be used to perform maskless lithography in mass quantities. Maskless lithography can write finer features by rastering a nanometer-sized beam or probe to generate surface patterns and has been applied to niche applications such as device prototyping and low-volume production. Among all maskless methods, electron beam lithography can provide high resolution beyond the 10-year industry roadmap. Electron-beam lithography also has the highest scanning speed. This technology could be used for top-down nanomanufacturing methods to carry on the trends of ever decreasing critical dimensions and ever increasing design complexities of semiconductor chips at a relatively low cost.

## **Advantages:**

## **Technology ID**

2015-PAN-67012

## **Category**

Semiconductors/Fabrication &  
Process Technologies  
Materials Science &  
Nanotechnology/Nanomaterials  
& Nanostructures

## **Authors**

Liang Pan  
Xianfan Xu

## **Further information**

Parag Vasekar  
[psvasekar@prf.org](mailto:psvasekar@prf.org)

## **View online**



- Focuses optical energy at nanoscale
- Perform maskless lithography in mass quantities
- Highest scanning speed
- Semiconductor chip design at a lower cost

Potential Applications:

- Semiconductor industry
- Further development of nanotechnology
- Photonics and biological systems

**TRL: 4**

**Intellectual Property:**

Provisional-Patent, 2015-06-07, United States | Utility Patent, 2016-06-07, United States | CON-Patent, 2018-09-11, United States | CON-Gov. Funding, 2020-10-19, United States

**Keywords:** Optical lithography, maskless lithography, electron beam lithography, massively parallel, nanoscale, semiconductor chips, nanomanufacturing, critical dimensions, high resolution, scanning speed