PURDUE INNOVATES | Office of Technology Commercialization

Embedded microchannel cooling in Semiconductor back-end-of-line

Novel microchannel cooling boosting performance and reliability in next-gen semiconductors and supercomputers.

Researchers at Purdue University have developed a novel cooling method to enable backside power delivery networks. Power Delivery Networks (PDNs) are parts of semiconductors designed to deliver power and reference voltage to the active devices within the die, or the small block of semiconducting material on which electrical circuits are fabricated. The traditional frontside power delivery network (FSPDN) results in competition for space between the power source and signal network. The backside power delivery network (BSPDN) promises large improvements over traditional FSPDN designs because of its ability to enhance system performance, maximize chip area utilization, improve power integrity, and simplify design complexity. However, BSPDN chip designs struggle to maintain proper cooling, risking self-heating due to their extremely thin substrate. Researchers at Purdue University have developed a novel method of tackling this issue. By embedding a two-layer microchannel cooling solution into already existing air gap structures that are process compatible with the Back-end-of-Line (BEOL) manufacturing process, this technology will significantly improve temperature reduction over traditional cooling methods while also controlling problematic pressure drops. Novel solutions such as this one will pave the way for next generation semiconductor manufacturing and supercomputer technologies.

Technology Validation:

In numerical simulations, the new BSPDN package structure reduced the junction temperature by a factor of three.

Advantages:

-Improved temperature and pressure control compared to traditional cooling methods

Technology ID
2024-WEI-70574

Category
Semiconductors/Packaging & Integration
Semiconductors/Thermal Management & Cooling Technologies

Authors
Tiwei Wei

Further information
Matt Halladay
MRHalladay@prf.org

View online

-Utilizes already-existing air gap structures, simplifying the manufacturing process

-Improves performance of next gen BSPDN semiconductors (enhance system performance, maximize chip area utilization, improve power integrity)

-Improves chip power, performance, and area (PPA)

Applications:

-Semiconductor manufacturing

-Supercomputer technology

TRL: 2

Intellectual Property:

Provisional-Patent, 2024-05-24, United States

Utility Patent, 2025-05-23, United States

Keywords: Backside power delivery network,Advanced semiconductor cooling,Microchannel cooling,Air gap thermal management,High-performance chip cooling,Next-gen semiconductor packaging,Thermal management for semiconductors,BEOL-compatible cooling,Power integrity enhancement,Semiconductor heat dissipation,Microfluidic cooling systems,Supercomputer thermal solutions,Chip performance optimization,Thermal design for electronics