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Backside Power Distribution in 3D Bonded Circuit

This novel 3D integrated circuit configuration improves power efficiency and thermal management in high-performance chips by exclusively using the heatsink-facing backside for power and ground routing with high-capacitance dielectrics.

As integrated circuits (ICs) become denser and more power-hungry, especially in AI and high-performance computing (HPC), designers face a critical challenge: how to deliver power efficiently while managing heat in 3D stacked architectures. Researchers at Purdue University have developed a novel configuration for 3D ICs that uses the backside of the heatsink-facing tier exclusively for power and ground routing. This enables the use of high-capacitance, thermally conductive dielectrics that are typically unsuitable for signal routing. Unlike current approaches that route power through the front side or compete with signal layers, this method isolates power delivery, improves thermal performance, and reduces power noise without sacrificing routing resources. Moreover, this approach could significantly improve power integrity and thermal management in next-generation AI and HPC chips, offering a scalable path for advanced 3D IC packaging.

Technology Validation: The concept is well-formulated with a clear physical rationale and integration path. Validation to date includes analytical modeling and design feasibility assessments. No fabrication or experimental data has been collected yet.

Advantages:

-Enables backside power routing without obstructing heat dissipation

-Uses high-capacitance dielectrics for power noise suppression

-Improves thermal conductivity compared to low-k signal dielectrics

-Reduces routing congestion by separating power and signal layers

-Compatible with pre-bonding fabrication on carrier wafers

Technology ID
2024-DUNG-70649

Category
Semiconductors/Packaging & Integration
Materials Science & Nanotechnology/Thermal Management Materials & Solutions
Semiconductors/Thermal Management & Cooling Technologies

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Applications:

-AI training accelerators

-High-performance computing (HPC) processors

-Advanced 3D IC packaging platforms

-Foundry-level process integration

-Data center and defense electronics

TRL: 3

Intellectual Property:

Provisional-Patent, N/A, United States

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Keywords: 3D integrated circuits, backside power routing, AI training accelerators, high-performance computing, HPC processors, power noise suppression, advanced 3D IC packaging, thermal management, thermally conductive dielectrics, foundry-level process integration, 3D ICs, advanced interconnects, AI chips, backside power delivery, Computer Technology, Electrical Engineering, high-capacitance dielectric, HPC packaging, hybrid copper bonding, Thermal Management, TSV