

A Novel Copper Microporous-Assisted Bonding Method for Fine-Pitch Cu/Sn Microbump 3D Interconnects

A novel bonding method utilizing copper microporous layers within Sn-based solder microbumps enhances thermal conductivity and mechanical performance for fine-pitch 3D semiconductor interconnects.

With the increasing demand for emerging and growing computing needs, three-dimensional (3D) integration with fine-pitch, high-density interconnections and multi-chip stacks is very promising in the future. The vertical 3D stacking provides shorter electrical interconnect length, leading to reduced power consumption and increased operating frequencies in electronic systems. Microbump bonding, commonly utilized in die-level platforms (die-to-die, die-to-interposer, or substrate), typically employs pitches ranging from 30-50 microns. However, soldering microbumps face issues such as void formation during reflow, which compromises bonding quality and reliability. Porous metal infiltration can lead to uneven metallurgical bonding, causing stress concentrations and mechanical failures. Additionally, traditional solder joints are vulnerable to electromigration, especially in smaller bump sizes. This leads to material migration and interconnect failure, which reduces overall device reliability. Moreover, the relatively low thermal conductivity of the bonding layer interface may still limit heat conduction within the 3D stacking system.

Purdue researchers have developed a novel method to improve chip power of semiconductors that is compatible with traditional low-temperature BEOL processes. This method incorporates micro/nanoscale porous copper inverse opals (CIO) within Sn-based solder microbumps. The researchers fabricated CIO-based microporous structures with a 3-micrometer pore size on a 100-micrometer diameter Cu bump, achieving a targeted thickness ranging from 3 to 5 micrometers. By incorporating Cu microporous layers, the bonding method reduces the formation of unintentional voids and ensures a better bonding between the Cu and Sn layer. This method reduces the stress at the bonding interface, resulting in enhanced thermal conductivity by several factors at the bonding interface. Furthermore,

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Category

Semiconductors/Packaging & Integration

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Management Materials & Solutions

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researchers were able to see a decrease in the maximum temperature by more than 20% for uniform heat flux as well as heat map cases. The developed method shows promise in improving electronic components and has potential commercial applications in the microelectronic packaging industry.

Related Publications:

K. Wang, S. Lyu and T. Wei, "A Novel Copper Microporous-Assisted Bonding Method for Fine-Pitch Cu/Sn Microbump 3D Interconnects," 2024 IEEE 74th Electronic Components and Technology Conference (ECTC), Denver, CO, USA, 2024, pp. 563-570, doi: 10.1109/ECTC51529.2024.00095.

Technology Validation:

- Finite Element Analysis was performed to study the thermal performance of chips
- Maximum chip temperatures were determined for the developed method

Advantages:

- Increased thermal conductivity within semiconductor chips
- Increased mechanical performance within semiconductor chips

Applications:

- Semiconductor chips
- Electronic systems

TRL: 4

Intellectual Property:

Provisional-Patent, 2024-05-24, United States

Utility Patent, 2025-05-20, United States

Keywords: 3D integration, microbump bonding, fine-pitch interconnects, porous copper inverse opals (CIO), semiconductor chips, electronic systems, enhanced thermal conductivity, high-density interconnections, low-temperature BEOL processes, microelectronic packaging, Cooling, Heat Transfer, Mechanical Engineering, Micro & Nanotechnologies, microelectronics, semiconductor, thermal interface, thermal interface

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