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A method for measuring high thermal conductance across deeply buried interfaces in advanced semiconductor packaging

Non-destructive laser-optical sensing measures deeply buried thermal interface resistance in advanced semiconductor packaging with low cost and no prep.

Understanding interfacial thermal resistivity is important for the design of advanced semiconductor packaging, but current techniques to characterize thermal resistivity of deeply buried interfaces in advanced semiconductor packaging are limited in resolution and require extensive sample preparation. Researchers at Purdue University developed a non-destructive approach to measure thermal contact resistance within a few millimeters below the exposed surface of a sample. Leveraging laser-based heating and optical temperature sensing, these fast and versatile measurements can probe deep interfaces without destroying the sample. Low-cost lasers and consumer-grade detectors are used, enabling affordable and accurate technology without the need for additional precise alignment elements. Additionally, unlike existing techniques, minimal sample preparation like cross sectioning the sample is required.

Technology Validation:

The 1D gradient approach was demonstrated experimentally across a range of materials and contact resistances. In addition to measuring interface resistances, this technique can probe the bulk materials with high accuracy across a wide range of materials ranging from thermal insulators to highly conductive materials, spanning a range of 0.1 to 2000 W mâˆ’1 Kâˆ’1.

Advantages:

-Fast, optical measurement

-Non-destructive

-Low cost

Technology ID

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Category

Semiconductors/Devices & Components
Materials Science & Nanotechnology/Advanced Functional Materials
Materials Science & Nanotechnology/Materials Testing & Characterization Tools

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View online

-Avoids sample preparation

-Utilizes off-the-shelf equipment

Applications:

-System-on-chip (SoC)

-Semiconductor packaging technologies

-Modern electronics packages

Publications:

Aalok Gaitonde. PhD Dissertation. https://hammer.purdue.edu/articles/thesis/METROLOGY_DEVELOPMENT_FOR_THERMAL_CHALLENGES_IN_ADVANCED_SEMICONDUCTOR_PACKAGING/27095515

Feasibility Assessment of Metrologies for Thermal Resistance Characterization of Deeply Buried Interfaces between Bonded Silicon Layers. 2023 22nd IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm). https://doi.org/10.1109/ITherm55368.2023.10177615

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Utility Patent, 2025-05-28, United States

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